

FIG. 1A

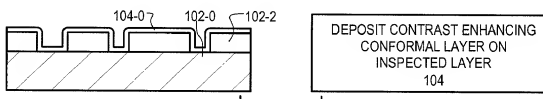


FIG. 1B

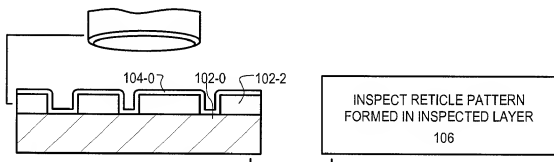


FIG. 1C



FIG. 2A

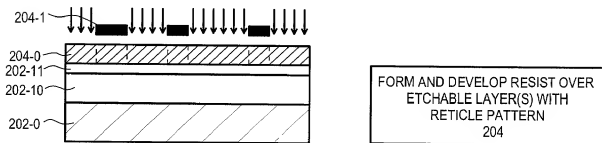


FIG. 2B

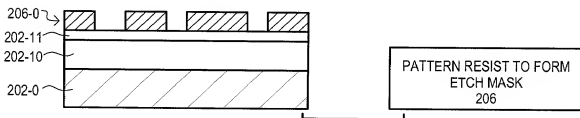


FIG. 2C

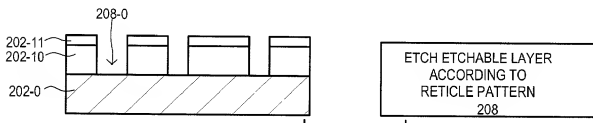


FIG. 2D

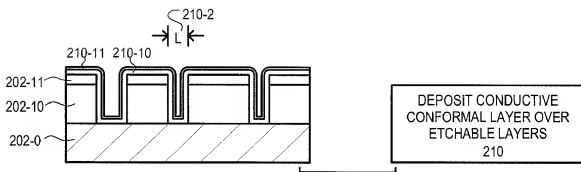


FIG. 2E

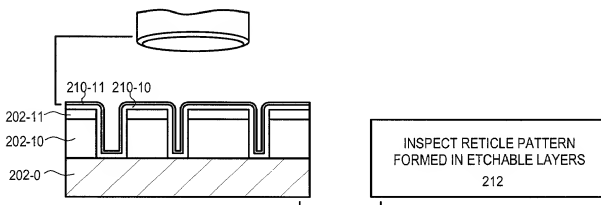
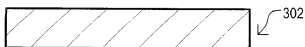
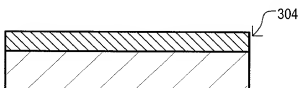


FIG. 2F



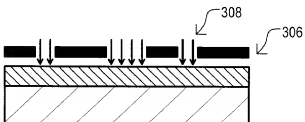
WAFER PREPARATION

FIG. 3A



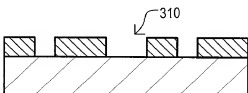
DEPOSIT RESIST

FIG. 3B



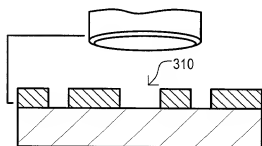
EXPOSE RESIST

FIG. 3C



DEVELOP RESIST

FIG. 3D



INSPECT RETICLE PATTERN
FORMED IN RESIST LAYER

FIG. 3E